NON OVERLAPPING CLOCKS FOR SWITCHED CAPACITOR CIRCUITS

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Abstract: Switched capacitor techniques are very popular for implementation of Mixed Signal blocks in CMOS VLSI. Non-Overlapping Clock (NOC) generator is one of the key blocks in the implementation of switched capacitor circuits. Standard NOC generator circuits available in the literature uses delay circuits realized using simple inverters connected in a chain. By using inverter chain delay generated is very small so to generate larger delay it requires larger numbers of inverters. This affects the area and power budget of the design. In this work it is proposed to use inverters in inverted form to realize significant delay with less number of transistors. Simulation results suggest that the proposed circuit will be area and power efficient as compared to the conventional NOC circuits.

Keywords: NOC (Non-overlapping clocks), SC (Switched capacitor circuits), Inverted inverter

I. INTRODUCTION

In Analog and Mixed Signal design Switched capacitor (SC) circuits are the most default standard for circuit implementation in CMOS VLSI. SC circuits are very important as analog signal processing blocks such as switched capacitor integrators, filters and voltage comparators. Mixed signal applications like Analog to Digital Converter (ADC), Sigma Delta Modulators and Sampled Analog Architectures employ Switched Capacitor circuits extensively. SC circuits offer several advantages such as high accuracy, low power consumption and better temperature invariance. To implement any SC block, it is required to charge and discharge the capacitor through switches by means of a non-overlapping clock. For implementation of NOC generator, there are several standard designs based on the delay element realized through chain of inverters and a few NAND/NOR gates. To achieve larger delay, some technique demands more number of inverters which in turn consumes more power and area. To reduce the number of stages for a given delay, use of transmission gates (TG) between two inverters is also proposed. In this kind of design, the delay of combined block (Inverter + TG) is more than that of two inverters of same size mainly due to the larger input capacitance seen by the inverter. However, two parallel charging (discharging) paths through NMOS and PMOS combination effectively reduces the delay than expected.
In this paper use of inverter in combination with an Inverted inverter (altering the position of nMOS with pMOS and vice versa) as a unit delay element. As mentioned, the delay of this combination is more for two reasons. First, the signal swing of the inverted inverter is not rail to rail but less by VT on both sides. Therefore, the effective voltage swing of the inverted inverter output is between $V_{DD} - VTn$ to $|VTp|$. However, the voltage swing will be less if the input voltage to the inverted inverter has less than full swing, which will be the case when number of such blocks is connected as a chain. Thus, switching delay is increased by not allowing the inverter transistors to turn off during the entire excursion of the signal. Therefore, when NMOS transistor of the inverter is applied high voltage ($V_{DD} - VTn$), both pull-down path and pull-up path is active. Moreover, the nMOS transistor will be getting less gate source voltage, which results less drain current to pull the output to low state. Eventually, the discharging will be slower than that of a normal inverter with input VDD. Using similar logic, it is evident that pull-up time will also be slower than that of a normal inverter with logic 0 input.

![Figure 1: Delay chain (a) Cascaded inverter, (b) Inverter with inverted inverter](image)

**II. DELAY OF INVERTED INVERTER**

The inverted inverter can be viewed as similar to pass gate, where the drain terminal of nMOS is input, which is now connected to $V_{DD}$ and the switch is activated by a weak logic high signal. Also, the drain terminal of PMOS is connected to ground and the switch is activated by weak logic low signal. If we assume that the weak 1 (generated at the output of the inverter) is represented by ($V_{DD} - x$), the output of the pass gate will be ($V_{DD} - x - VTn$), where $VTn$ represents the threshold voltage of the inverter with body voltage $\sim V_{DD} - VTn$.

Similarly, the output voltage of the pass gate when pMOS pass transistor is on will be weak 0 and is $\sim VTp$. Here also, $|VTp|$ represents the threshold voltage of the pMOS transistor with substrate bias of $VTp$ which will be quite higher than $VTpo$.

**III. NON-OVERLAPPING CLOCK GENERATOR**
To generate non-overlapping clocks with better delay, the block diagram is shown in figure. Here the NOR based circuit and for delay chain cascaded inverted inverter is used. As mentioned earlier inverted inverter has larger delay than cascaded inverter with same transistor count. Also by increasing stages we can achieve larger delay.

### IV. SIMULATION RESULTS

![Non Overlapping Clock Generator Diagram](image-url)

Figure 3: Non overlapping clock generator using inverter chain
Figure 4: Non overlapping clock generator using inverted inverter

Figure 5: Non overlapping clock signals using inverted inverter
TABLE I: Delay comparison of non-overlapping clock generator using different architectures

<table>
<thead>
<tr>
<th>Transistor Count</th>
<th>Cascaded Inverter</th>
<th>Inverter with Inverted inverter</th>
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</thead>
<tbody>
<tr>
<td>Delay</td>
<td>153ps</td>
<td>5.111ns</td>
</tr>
</tbody>
</table>

TABLE II. Comparison Table

<table>
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<th>This work</th>
<th>[2]</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90nm</td>
<td>180nm</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Delay</td>
<td>5.111ns</td>
<td>7.2ns</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In this paper we have used inverter in combination with inverted inverter to generate non-overlapping clock signals. Use of this block is generates larger delay compared to inverter chain. By using this, delay between two non-overlapping clock is 5.111ns in 90nm technology.

REFERENCES