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Simulation of Phase Locked Loop Circuit in Non-Linear Load

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ABSTRACT

Nonlinear load produces the harmonics in the supply system and deteriorate voltage and current wave shape. Thisdistortion can be minimized by use of PLL.This paper presents the effective solution to reduce harmonics by using phase locked loop (PLL). This paper contains simulation of PLL in three phase system. Simulation results are also shown in the paper.

KEY WORDS: *Phase locked loop, P-I controller, fictitious power*

INRODUCTION

From past few years the use of nonlinear load has been increased in our daily life. This nonlinear load produces harmonics in the supply system voltage and load current. Thus we are getting distorted voltage and current. This harmonics can be reduced by using Phase Locked Loop. PLL continuously track fundamental frequency in distortion condition

PHASE LOCKED LOOP

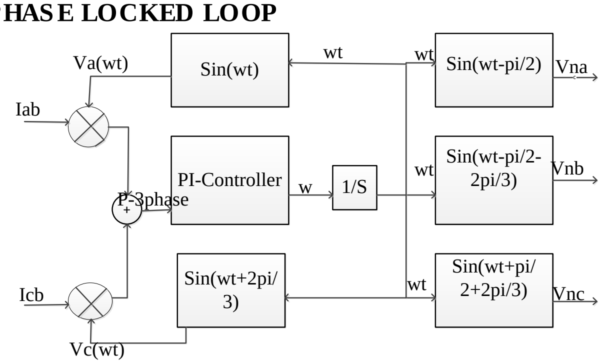

Fig.1 Phase locked loop

The PLL circuit tracks continuously the fundamental frequency of the load current. PLL circuit is almost insensitive to unbalances and distortions. PLL circuit determines the frequencyand phase angle of the fundamental positive sequence component of the load currents Ia, Ib, Ic. This circuit is very effective even under high distorted and unbalanced input.

The algorithm is based on the instantaneous active three phase power expression

$$p3\phi = v_a i_a + v_b i_b + v_c i_c$$
$$= v_a i_a - v_a i_b - v_c i_b + v_c i_c$$
$$= i_{ab} v_a + i_{cb} v_c \quad \text{Eq. (1)}$$

Note that the relation va + vb + vc = 0 in (1). As no current is measured from the power circuit, it is difficult to understand how the PLL circuit works. The voltage feedback signals of Fig.1 va(ωt) = sin(ωt) and vc(ωt) = sin(ωt+2π/3) are built up by the PLL circuit, by using the time integral of output ω of the PI Controller. Note that they have unity amplitude and vc(ωt) leads 120º va(ωt). Thus, they represent a feedback from a positive-sequence component at frequency ω. The PLL circuit can reach a stable point of operation only if the input p3φ of the PI Controller has zero average value and has minimized low frequency oscillating portions.The average three-phase power (P3φ= P'3φ), in terms of phasors, is given by

$P_{3\varphi} = p'_{3\varphi} = 3V_{+1}I_{+1}\cos\varphi,$ Eq. (2)

a stable point of operation is found only if ω equals the system frequency and the feedback signal corresponding to auxiliary voltage signal $v_a(\omega t)$ becomes orthogonal to the fundamental positive-sequence component of the measured load current i_a.

However, if the point where $i_a$leads the feedback signal $v_a(\omega t)$ 90º is reached, this is still an unstable point of operation.

At this point, an eventual disturbance that slightly increases the system frequency (the frequency of $i_{ab}$and i_{cb}) will make the current phasor(I_{+1}) to rotate faster than the voltage phasor built up from the feedback voltage signals $v_a(\omega t)$ and $v_c(\omega t)$. Hence, the displacement angle between i_a and $v_a(\omega t)$, given by cosφ becomes greater than 90º.This results in negative average input ($p'_{3\varphi} < 0$) and consequently to a decreasing output ω, making the phase angle between $i_a$and $v_a(\omega t)$ even greater. This characterizes an unstable point of operation. Thus, the PLL has only one stable point of operation, that is the feedback signal $v_a(\omega t)$ leading 90º the load current i_a. Now, if the same disturbance is verified, the displacement angle between the voltage and current phasors will be reduced and the average power in (2) will be positive. This will make the voltage phasor to rotate faster, keeping the orthogonality (lagging currents) between the generated V'_{+1} $[v_a\omega t)]$ and the measured $I._{+1}$. This fundamental characteristic of the PLL circuit shown in Fig.1 can be exploited to compose the needed sinusoidal functions. If $v_a(\omega\, t)$ = $\sin(\omega t)$ leads 90º the fundamental positive sequence component of the load current, then, $v_{Na}(\omega\, t)$ = $\sin(\omega\, t - \pi/2)$ must be *in phase* with $I._{+1}$. In other words, the signals v_{Na}, v_{Nb} and $v_{Nc}$are sinusoidal time functions with unity amplitude, have the same frequency, and are in phase with the fundamental positive-sequence component of the measured load current.

PI CONTROLLER

P-I controller is mainly used to eliminate the steady state error resulting from P controller. However, in terms of the speed of the response and overall stability of the system, it has a negative impact. This controller is mostly used in areas where speed of the system is not an issue. Since P-I controller has no ability to predict the future errors of the system it cannot decrease the rise time and eliminate the oscillations. If applied, any amount of I guarantees set point overshoot.

It is a proportional gain in parallel with an integrator, both in series with a lead controller. The proportional gain provides fast error response. The integrator drives the system to a 0 steady-state error.
The transfer function of P-I controller is given by expression:

$G(s)=Kp+(Ki/s)$ Eq. (3)

SIMULATION RESULTS

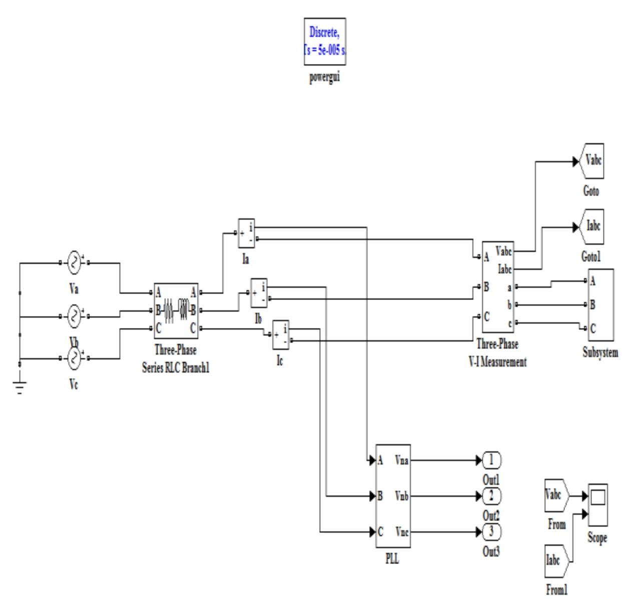

Fig. 2 Simulation Diagram

Subsystem of nonlinear load

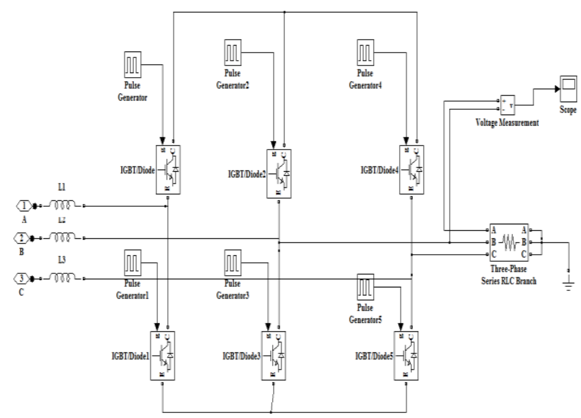

Fig.3 Nonlinear Load

Fig.2 shows the simulation model.Fig.3 shows the subsystem of nonlinear load. Here three phase IGBT/Diode is used as nonlinear load. Pulse generator is used for generating the gate signals.

Fig.4 shows simulation of Phase Locked Loop circuit. The inputs are three phase currents A, B, C sensed from Fig.1. Fig.5 shows the output waveforms.

Subsystem of PLL

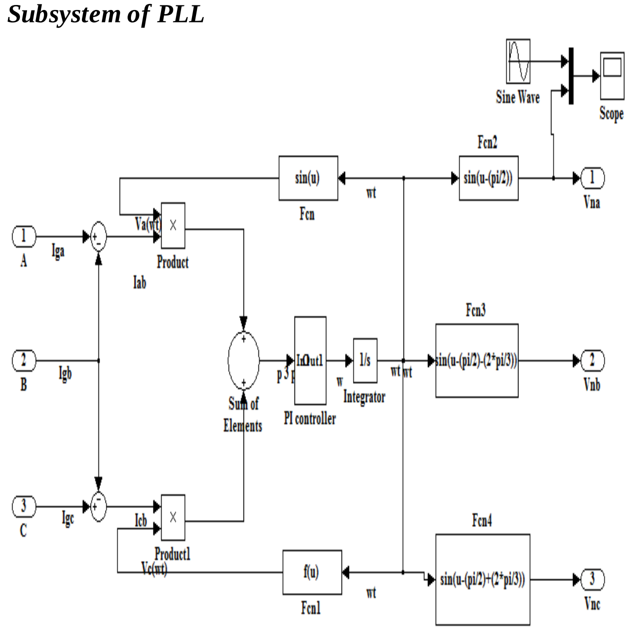

Fig. 4 Phase locked loop

PLL OUTPUT WAVEFORM

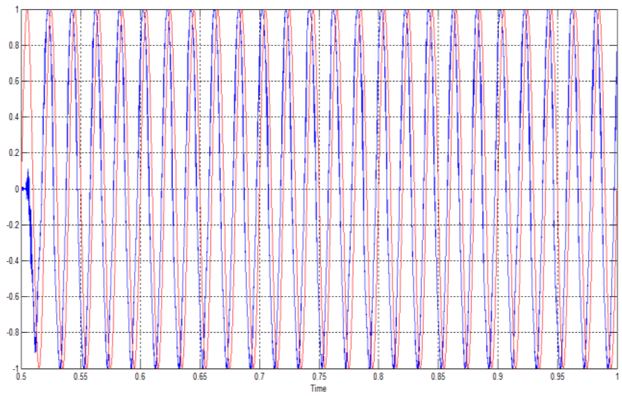

Fig. 5 Voltage and Current waveform

CONCLUSION

In this paper simulation of phase locked loop circuit is done. It continuously track fundamental frequency in distortion condition. Positive sequence component compare with sine wave which is shown in figure. So that fundamental frequency can be track.

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